IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) An ESD protection circuit comprising:

a first pad which is used as an external connection terminal to be connected to a semiconductor integrated circuit;

a second pad which is used as an external connection terminal to be connected to the semiconductor integrated circuit;

a clamp circuit connected between the first pad and the second pad; [[and]]

a control circuit which is configured to control the clamp circuit; and

a third pad which is connected to the control circuit,

wherein the control circuit is configured to render the clamp circuit conducting when the same potential as applied to the second pad is applied to the third pad before the semiconductor integrated circuit is incorporated into an end product, and to render the clamp circuit non-conducting when a predetermined potential is applied to the third pad after the semiconductor integrated circuit is incorporated into the end product.

2. (Original) The ESD protection circuit according to claim 1, wherein the clamp circuit includes a switch element which is rendered to be conducting or non-conducting in accordance with a control signal output from the control circuit.

3. (Original) The ESD protection circuit according to claim 1, wherein the clamp circuit includes an inverter circuit which receives a control signal from the control circuit, and a switch circuit which is turned on or off by an output signal of the inverter circuit.

4. (Original) The ESD protection circuit according to claim 3, wherein the inverter circuit comprises a first MOS transistor of a first conductivity type, whose source is connected to the first pad and whose gate is connected to receive the control signal from the control circuit, and a second MOS transistor of a second conductivity type, whose drain is connected to a drain of the first MOS transistor, whose source is connected to the second pad, and whose gate is connected to receive the control signal from the control circuit.

5. (Original) The ESD protection circuit according to claim 3, wherein the switch circuit comprises a third MOS transistor of the second conductivity type, whose drain is connected to the first pad, whose source is connected to the second pad, and whose gate is connected to an output terminal of the inverter circuit.

6. (Original) The ESD protection circuit according to claim 4, wherein the switch circuit comprises a third MOS transistor of the second conductivity type, whose drain is connected to the first pad, whose source is connected to the second pad, and whose gate is connected to an output terminal of the inverter circuit.

7. (Original) The ESD protection circuit according to claim 3, wherein the switch circuit comprises an NPN bipolar transistor whose collector is connected to the first pad, whose emitter is connected to the second pad and whose base is connected to an output terminal of the inverter circuit.

8. (Currently Amended) The ESD protection circuit according to claim 3, wherein the switch circuit comprises a PNP bipolar transistor whose ~~emitter~~ collector is connected to the

first pad, whose ~~collector~~ emitter is connected to the second pad and whose base is connected to an output terminal of the inverter circuit.

9. (Original) The ESD protection circuit according to claim 3, wherein the switch circuit comprises a thyristor whose anode and cathode are connected between the first pad and the second pad, and a trigger circuit which supplies a trigger current to the thyristor to turn on or off the thyristor.

10. (Canceled)

11. (Currently Amended) The ESD protection circuit according to claim 9, wherein the trigger circuit comprises a ~~fourth~~ MOS transistor of a second conductivity type, whose ~~source~~ one end of the current path is connected to the first pad and whose gate is connected to an output terminal of the inverter circuit, and a ~~first~~ resistor element which is connected at one end to ~~a drain~~ another end of the current path of the ~~fourth~~ MOS transistor and at the other end to the second pad.

12. (Original) The ESD protection circuit according to claim 1, wherein the control circuit renders the clamp circuit conducting when no power is supplied to the semiconductor integrated circuit, and renders the clamp circuit non-conducting when power is supplied to the semiconductor integrated circuit.

13. (Canceled)

14. (Currently Amended) The ESD protection circuit according to claim ~~13~~ 1, wherein the control circuit includes a load circuit connected at one end to the third pad and at the other end to a first potential source which generates the predetermined potential.

15. (Currently Amended) The ESD protection circuit according to claim 14, wherein the load circuit includes a ~~second~~ resistor element.

16. (Currently Amended) The ESD protection circuit according to claim 1, wherein the control circuit comprises a programmable circuit which renders the clamp circuit conducting before the semiconductor integrated circuit is incorporated into an end product, and renders the clamp circuit non-conducting after ~~is programmed in accordance with whether a semiconductor chip including~~ the semiconductor integrated circuit is ~~has been~~ incorporated into ~~an~~ the end product~~, and renders the clamp circuit conducting or non-conducting in accordance with data programmed in the programmable circuit~~.

17. (Currently Amended) The ESD protection circuit according to claim 16, wherein the programmable circuit comprises a fuse circuit which has a fuse element whose one end is connected to the third pad ~~that is cut after the semiconductor chip is incorporated into the end product~~, and the semiconductor chip has a fourth pad ~~and fifth pads~~ which is connected to the other end of ~~supply a current to~~ the fuse element, a voltage is supplied between the third and fourth pads to cut the fuse element after the semiconductor chip is incorporated into the end product.

18. (Currently Amended) The ESD protection circuit according to claim 17, wherein the fuse circuit includes a ~~third~~ first resistor element which is connected between one end of

the fuse element and a first potential source that generates a first potential, and a ~~fourth~~ second resistor element which is connected between the other end of the fuse element and a second potential source that generates a second potential.